20. The high voltage MOS transistor of claim ~~19~~ 1 having one channel conductivity type in combination with a ~~complimentary~~ complementary high voltage MOS transistor of an opposite channel conductivity type combined on the same chip and isolated from each other.

21. The high voltage MOS transistor of claim ~~19~~ 1 combined on the same chip with a low voltage CMOS implemented device.

22. The combination of claim 21 further including,

a ~~complimentary~~ complementary high voltage MOS transistor, and

a ~~complimentary~~ complementary low voltage CMOS implemented device on the same chip and isolated from each other.

23. A high voltage MOS transistor comprising:

a semiconductor substrate of a first conductivity type having a surface,

a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,

a source contact connected to one pocket,

an extended source region of the second conductivity type extending laterally each way from the source contact pocket to surface-adjoining ~~position~~ positions,

a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended source region between the surface-adjoining positions,

said top layer and said substrate being subject to application of a reverse-bias voltage,

a drain contact connected to the other pocket,

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an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,

a layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,

said top layer of material and said substrate being subject to application of a reverse-bias voltage,

an insulating layer on the surface of the substrate and covering at least that portion between the nearest surface-adjoining positions of the extended source region and the extended drain region, and

a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the nearest surface-adjoining positions of the extended source region and the extended drain region, said gate electrode controlling by field-effect the current flow thereunder through the channel.

Amend the claims as follows:

Claim 6, line 1, change "5" to --19--; and

Claim 7, line 1, change "5" to --19--.

REMARKS

The specification has been amended to correct minor errors and to provide an antecedent basis in the specification for epitaxial layer and epi-island mentioned in former claims 11 and 13.

This invention relates to high voltage, metal oxide semiconductor transistors of the field effect type. There is a need for more efficient transistors which can be made as either discrete or integrated devices of either n-channel or p-channel conductivity. The

integrated devices should be easily combined with low voltage (five volt) control logic on the same chip. Devices of opposite conductivity should be combinable in a complimentary manner on the same chip. Such transistors, with modifications, should be capable of source-follower applications.

The applicant has disclosed a novel and unobvious high voltage MOS transistor having a low threshold voltage that is compatible with five volt control logic and a low ON-resistance. This transistor can be made as either discrete or integrated devices of either n-channel or p-channel conductivity. The high voltage MOS transistors can be modified for source-follower applications by providing both extended source regions and extended drain regions. These transistors are formed on a substrate of a first conductivity type having a surface. A pair of laterally spaced pockets of semiconductor material of a second conductivity type are provided within the substrate and adjoining the substrate surface. A source contact is connected to one pocket and a drain contact is connected to the other pocket. An extended drain region of a second conductivity type extends laterally each way from the drain pocket to surface-adjoining positions. A layer of material of the first conductivity type is provided on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions. The top layer of material and the substrate are subject to application of a reverse-bias voltage. None of the cited references show such structure.

Colak, U.S. Patent No. 4,626,879, shows a DMOS transistor suitable for source follower applications. This device has a substrate with three epitaxial layers formed thereon. A surface-adjoining channel region is diffused into the epitaxial layers and a source region is diffused into the channel diffusion above the channel region. A drain region is diffused into the top epitaxial layer. An extended drain

region is formed from a portion of the top epitaxial layer between the drain region and the channel region. The top and bottom epitaxial layers are interconnected, and the bottom layer may operate as a parallel extended drain region between the connection points. The intermediate epitaxial layer may operate as an extended drain region in a dual-gate/dual-drain structure wherein all three epitaxial layers contribute to device conductivity for achieving optimum normalized "ON" resistance.

Thomas, U.S. Patent No. 4,628,341 shows an integrated circuit structure that includes both low-voltage n-channel and p-channel MOS transistors and high voltage n-channel and p-channel MOS transistors.

The claims are now clearly distinguished from the cited references. New claim 19 recites "an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions, a layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions". When high voltage n-channel and p-channel devices are combined on the same chip with low voltage control logic, this structure isolates the devices from each other. Claim 19 also provides for a pair of laterally spaced source and drain contact pockets within the substrate as is customary for conventional MOS transistors and is thus, distinguished from DMOS devices which require a higher threshold voltage. The structure of claim 19 enables a lower threshold voltage, compatibility with five volt control logic, and eliminates the need for an additional power supply and interface circuit.

Claims 20-22 and claims 6-7 depend directly or indirectly from claim 19 and thus, can be distinguished for the same reasons as claim 19.

Claim 23 is directed to the transistor, shown in Fig. 5 of the drawings, that has been modified for source-follower applications by providing both extended source and drain regions. Top layers cover intermediate portions of the extended source and drain regions. The top layers and substrate are subject to application of a reverse-bias voltage.

Accordingly, claims 6-7 and 20-23 are patentably distinct from the cited references and allowance of these claims is requested.

If the Examiner is of the opinion that a telephone conference with applicant's attorney would expedite matters, such a conference is invited.

Respectfully submitted,

Reg. No. 22,611

By _____
Thomas E. Schatzel

LAW OFFICES OF THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard, Suite 201
Santa Clara, California 95054
Telephone: (408) 727-7077

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 4-7-88
(Date of Deposit)

Thomas E. Schatzel
Name of applicant, assignee or Registered Rep.

Signature

4/7/88
Date

Serial No.: 07/041,994
Filed: 4-24-87
Attnys. Docket No.: SS-520-01

PATENT

CONDITIONAL PETITION FOR EXTENSION OF TIME

If any extension of time for this response is required applicant requests that this be considered a petition therefor.

Status

This application is on behalf of:

___ other than a small entity

____ verified statement attached

__X__ small entity

__X__ verified statement already filed

Payment of fees

__X__ The Commissioner is hereby authorized to charge any additional fees as set forth in 37 C.F.R. 1.16 and 1.17 which may be required or credit any overpayment to Account No. 19-0310. A duplicate of this transmittal is attached.

NOTE: Please ____also
__X__ do not charge issues fees under 37 C.F.R. 1.18 to Account No. 19-0310.

Reg. No. 22,611

Attorney for Applicant

Telephone: (408) 727-7077

Law Offices of Thomas E. Schatzel
A Professional Corporation
3211 Scott Boulevard, Suite 201
Santa Clara, California 95054

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 4-7-88 (Date of Deposit)

Thomas E. Schatzel
Name of applicant, assignee, or Registered Rep.

Signature 4/7/88 Date

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
07/041,994	04/24/87	EKLUND K	SS-520-01

THOMAS E. SCHATZEL
3211 SCOTT BLVD., STE. 201
SANTA CLARA, CA 95054-3093

EXAMINER	
JACKSON JR, J	
ART UNIT	PAPER NUMBER
253	4

DATE MAILED: 06/17/88

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☒ Responsive to communication filed on 4/11/88 ☒ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), ____ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449
4. ☐ Notice of Informal Patent Application, Form PTO-152
5. ☐ Information on How to Effect Drawing Changes, PTO-1474
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 6, 7, 19-23 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 6, 7, 19-23 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings which are acceptable for examination purposes until such time as allowable subject matter is indicated.
8. ☐ Allowable subject matter having been indicated, formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. These drawings are ☐ acceptable; ☐ not acceptable (see explanation).
10. ☐ The ☐ proposed drawing correction and/or the ☐ proposed additional or substitute sheet(s) of drawings, filed on _____, has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved. ☐ disapproved (see explanation). However, the Patent and Trademark Office no longer makes drawing changes. It is now applicant's responsibility to ensure that the drawings are corrected. Corrections MUST be effected in accordance with the instructions set forth on the attached letter "INFORMATION ON HOW TO EFFECT DRAWING CHANGES", PTO-1474.
12. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

PTOL-326 (Rev. 7-82) EXAMINER'S ACTION

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless-

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 19, 6, 7 are rejected under 35 U.S.C. 102 (e) as anticipated by or, in the alternative, under 35 U.S.C. 103 as obvious over Colak.

Claim 19 still does not distinguish over Colak. See figures 1, 2B and 2C of Colak where 22 and 24 define "pockets", layers 18 and 14 form an "extended drain" which extends to the surface "each way" from the drain contact 24, layer 16 defines a layer of material of first conductivity type "on top of" extended drain layer 14, and layer 16 and substrate 12 are subject to application of a reverse bias voltage during operation of the device. Note that layer 16 is connected to the source and the substrate is reverse biased through SS. Thus claim 19 does not distinguish over Colak. Claim 5 is undistinguishing since Colak teaches a layer 16 thickness of 2 micron for 400 V operation, however, for lower voltage operation design layer 16 would be thinner, and 1 micron thickness is thus an obvious design variant to the artist. Similarly, to the artist, the design of claim 7 is obvious in view of Colak who teaches $10^{16}/cm^3$ for layer 16.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Claims 20-23 are rejected under 35 U.S.C. 103 as being unpatentable over Colak in view of Thomas.

As stated in the previous rejection, Thomas shows that high voltage fet devices (as Colak) are advantageously formed complementary and also integrated with low voltage devices. Hence claims 20-22 are obvious.

Claim 23 is rejected under 35 U.S.C. 103 as being unpatentable over Sze.

Colak teaches punch through and avalanche protection layer 16 for a DMOS device. To one of ordinary skill it would have been obvious to practice the teachings of Colak in other MOS devices as ordinary fets as shown in Sze. Note figures 3, 51 or 52 of Sze where the source or drain are structurally similar and their function is dependent on the particular voltage applied. Hence, to the artist it would be obvious to apply the

teachings of Colak to symmetrical ordinary fets as shown in Sze to provide higher voltage operation.

Applicant's arguments filed April 11, 1988 have been fully considered but they are not deemed to be persuasive.

Applicant's argument that Colak does not show a drain "extending laterally each way" from the drain is not convincing as shown in the above rejection.

Clearly there is drain material 18 on each side of pocket 24.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, THIS ACTION IS MADE FINAL. See MPEP 706.07(a).

Applicant is reminded of the extension of time policy set forth in 37 CFR 1.136(a). The practice of automatically extending the shortened statutory period an additional month upon the filing of a timely first response to a final rejection has been discontinued by the Office. See 1021 TMOG 35.

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 CFR 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. Jackson whose telephone number is (703) 557-4824.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 557-3311.

J. Jackson:klw

6-15-88

(703) 557-4824

ANDREW J. JAMES
SUPERVISORY PATENT EXAMINER
GROUP ART UNIT 253

TO SEPARATE, H[illegible]D TOP AND BOTTOM EDGES, SNAP-APART AND D[illegible]CARD CARBON

FORM PTO-892 (REV. 3-78)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NUMBER
NOTICE OF REFERENCES CITED		041994	253	4
		APPLICANT(S) Eklund		

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	A						
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG	PERTINENT PP. SPEC.
	L								
	M								
	N								
	O								
	P								
	Q								

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

R	Sze, Physics of Semiconductor Devices Wiley & Sons N.Y. ©1981 pp 431-438, 486-491 (14) (14)
S	
T	
U	

EXAMINER	DATE
J. Jackson	6/88

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05 (a).)

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT		ATTORNEY DOCKET NO.
07/041,994	04/24/87	EKLUND	K	SS-520-01

THOMAS E. SCHATZEL
3211 SCOTT BLVD., STE. 201
SANTA CLARA, CA 95054-3093

EXAMINER	
JACKSON JR, J	
ART UNIT	PAPER NUMBER
253	5

DATE MAILED:

EXAMINER INTERVIEW SUMMARY RECORD

08/11/88

All participants (applicant, applicant's representative, PTO personnel):

(1) Jack Edwards (3) Klas H. Eklund

(2) Thomas E. Schatzel (4) Jerome Jackson

Date of interview 10 August 1988

Type: ☒ Telephonic ☐ Personal (copy is given to ☐ applicant ☐ applicant's representative).

Exhibit shown or demonstration conducted: ☐ Yes ☒ No. If yes, brief description: _____

Agreement ☒ was reached with respect to some or all of the claims in question. ☐ was not reached.

Claims discussed: all

Identification of prior art discussed: Colak

Description of the general nature of what was agreed to if an agreement was reached, or any other comments: New amendments to the claims to be submitted distinguishing applicant's channel structure and surface adjoining layer 27 over Colak.

(A fuller description, if necessary, and a copy of the amendments, if available, which the examiner agreed would render the claims allowable must be attached. Also, where no copy of the amendments which would render the claims allowable is available, a summary thereof must be attached.)

Unless the paragraphs below have been checked to indicate to the contrary, A FORMAL WRITTEN RESPONSE TO THE LAST OFFICE ACTION IS NOT WAIVED AND MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW (e.g., items 1–7 on the reverse side of this form). If a response to the last Office action has already been filed, then applicant is given one month from this interview date to provide a statement of the substance of the interview.

☐ It is not necessary for applicant to provide a separate record of the substance of the interview.

☐ Since the examiner's interview summary above (including any attachments) reflects a complete response to each of the objections, rejections and requirements that may be present in the last Office action, and since the claims are now allowable, this completed form is considered to fulfill the response requirements of the last Office action.

Jerome Jackson Jr.
Examiner's Signature

PTOL-413 (rev. 1-81)

ORIGINAL FOR INSERTION IN RIGHT HAND FLAP OF FILE WRAPPER

6

#6

PATENT

HAND CARRIED TO PTO

Case Docket No. SS-520-01

Date August 12, 1988

In re application of: Klas H. Eklund

Serial No.: 07/041,994

Filed: April 24, 1987

For: HIGH VOLTAGE MOS TRANSISTORS

ATTN: BOX A.P.
COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

Sir:

Transmitted herewith is an Amendment After Final for the above application.

[x] No additional fee is required.

[ ] Additional fee calculated as follows:

CLAIMS AS AMENDED						
	Claims remaining after amendment		Highest number previously paid for	Present extra	Rate	Addtnl. Fee
Total Claims	_____	Minus	_____ =	_____ x	$12.00	= _____
Indep. Claims	_____	Minus	_____ =	_____ x	$34.00	= _____

Additional Fee Due $ _____

[x] A verified statement claiming small entity status x has been filed; _____ is attached. The fee due is fifty percentum of the above.

Fee Due $ _____

[ ] A check in the amount of $_____ is attached.

[x] Any additional fees may be charged to Deposit Account No. 19-0310. A duplicate of this transmittal is attached.

Respectfully submitted,

By _____
Reg. No.: 22,611

Attorney For Applicant

Law Offices of THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard Suite 201
Santa Clara, CA 95054
(408) 727-7077

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Klas H. Eklund

Serial No.: 07/041,994

Filed: : April 24, 1987

For : HIGH VOLTAGE MOS TRANSISTORS

Group Art Unit: 253

Examiner: J. Jackson, Jr.

Attorneys Docket No.: SS-520-01

ATTENTION: BOX A.F.

COMMISSIONER OF PATENTS
& TRADEMARKS
Washington, D.C. 20231

Date of this Paper:
August 12, 1988

AMENDMENT AFTER FINAL

In response to the U.S. Patent Office Action mailed June 17, 1988 (Paper No. 4), please amend this application as follows:

In the Claims

Claim 19, line 12, before "layer" insert --surface adjoining--;
line 22, before "region" insert --substrate--.

Claim 20, line 2, change "complimentary" to --complementary--.

Claim 22, line 2, change "complimentary" to --complementary--;
line 3, change "complimentary" to --complementary--.

Claim 23, line 9, delete "a";
line 10, change "position" to --positions--;
line 11, before "layer" insert --surface adjoining--;
line 18, delete "a";
line 20, before "layer" insert --surface adjoining--;
line 30, before "region" insert --substrate--.

REMARKS

The applicant appreciates the telephone interview on August 10, 1988, courteously granted by the Examiner.

Claim 19, as amended, now provides for an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions and a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions. The layer 16 of Colak is not surface-adjoining but is buried under layer 18. There is no layer of material of the first conductivity type on top of layer 18. Colak's layer 16 extends from beneath the drain contact pocket 24 to the channel region 20, and thus, is not between the drain contact pocket and the surface adjoining positions of the extended drain region.

Claim 19 also provides for the top layer of material and the substrate being subject to application of a reverse-bias voltage. Thus, the top layer and the substrate act as gates for controlling current flow through the extended drain region between the surface adjoining positions and the drain contact pocket. This structure can be considered a double-sided, junction-gate field-effect transistor (JFET). Colak shows a layer 14 intermediate a layer 16 and a substrate 12 that are subject to application of a reverse-bias voltage. Though this structure of Colak could be considered a double-sided JFET, layer 16 is not surface-adjoining as defined in claim 19. Colak's double-sided JFET is buried under layer 18 which is connected in parallel with layer 14 by semiconductor zones 16c, 16d. Layer 16 also acts as a gate for layer 18 so that layers 16 and 18 could be considered a single-sided JFET. Thus, the extended drain of Colak includes the single-sided JFET connected in parallel with the double-

sided JFET thereunder. Both the extended drain structure of claim 19 and Colak's drain structure have relatively high voltage capability. However, it is desirable to control the high voltage with relatively low voltage.

Claim 19 further provides for a substrate having a surface, an insulating layer on the surface of the substrate covering at least that portion between the source contact pocket and the nearest surface-adjoining position of the extended drain region, and a gate electrode on the insulating layer electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region. Thus, claim 19 is limited to a MOS or MOSFET structure, while Colak shows a D-MOS device. The MOSFET structure has a lower threshold voltage than a D-MOS device (0.7 volts compared to two - four volts for the D-MOS device) and thus, is directly compatible with five volt logic. D-MOS devices usually require an additional power supply of ten to fifteen volts for driving the gate. The MOSFET structure has less on-resistance and thus, further reduces the total on-resistance of the combined structure (MOSFET plus double-sided JFET).

Claim 19 is directed to the structural combination of a double-sided JFET and a MOSFET so that a high voltage transistor can be controlled with relatively low voltage. Thus, claim 19 is patentably distinct over Colak.

Claims 20-22 and claims 6-7 depend directly or indirectly from claim 19 and are thus patentably distinct from Colak for the same reasons as claim 19. While Thomas shows that high voltage FET devices are advantageously formed complementary and also integrated with low voltage devices, claims 20-22 are limited to transistors having the structure as defined in claim 19. This structure facilitates isolation of complementary high voltage devices and low voltage, C-MOS

implemented devices on the same chip. Isolation of the epitaxial layers shown by Colak from corresponding layers of a complementary device would be difficult.

Claims 6 and 7 include further limitations on the depth of the top layer and the doping density thereof. The depth is one-half or less than that disclosed by Colak for layer 16 and the doping density is at least five times greater. Furthermore, Colak's layer 16 is not similarly situated as the top layer of claim 19, and thus, is not comparable. Thus, claims 6 and 7 are patentably distinct from Colak for the same reasons as claim 19 and for the further limitations therein.

Claim 23 is directed to the transistor 63, shown in Fig. 5, that is suitable for source follower applications. This claim contains limitations similar to claim 19 for the MOSFET structure and the double-sided JFET about the drain contact pocket. It further includes structural limitations for a double-sided JFET about the source contact pocket. While the book by Sze discloses MOSFET structures having sources and drains that are similar to each other, such sources and drains are not similar to the double-sided JFET structures disclosed by the applicant and specifically claimed structurally in claim 23. Thus, claim 23 is patentably distinguished from Sze.

Should the Examiner be of the opinion that a telephone conference with applicant's attorney would be beneficial, he is invited to contact the undersigned at the number set out below.

Respectfully submitted,

Reg. No. 22,611

By _____
Thomas E. Schatzel

LAW OFFICES OF THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard, Suite 201
Santa Clara, California 95054
Telephone: (408) 727-7077

PATENT

CONDITIONAL PETITION FOR EXTENSION OF TIME

If any extension of time for this response is required applicant requests that this be considered a petition therefor.

Status

This application is on behalf of:

___ other than a small entity

____ verified statement attached

_x_ small entity

_x_ verified statement already filed

Payment of fees

_X_ The Commissioner is hereby authorized to charge any additional fees as set forth in 37 C.F.R. 1.16 and 1.17 which may be required or credit any overpayment to Account No. 19-0310. A duplicate of this transmittal is attached.

NOTE: Please ____also _X_ do not charge issues fees under 37 C.F.R. 1.18 to Account No. 19-0310.

Reg. No. 22,611

Attorney for Applicant

Telephone: (408) 727-7077

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3211 Scott Boulevard, Suite 201
Santa Clara, California 95054

7

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
07/041,994	04/24/87	EKLUND K	SS-520-01

THOMAS E. SCHATZEL
3211 SCOTT BLVD., STE. 201
SANTA CLARA, CA 95054-3093

EXAMINER	
JACKSON JR, J	
ART UNIT	PAPER NUMBER
253	7

DATE MAILED: 8-25-88
~~08/10/88~~

NOTICE OF ALLOWABILITY

PART I.

1. [X] This communication is responsive to Amend B 8/15/88
2. [X] All the claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice Of Allowance And Issue Fee Due or other appropriate communication will be sent in due course.
3. [X] The allowed claims are 6,7, 19-23
4. [ ] The drawings filed on _____ are acceptable.
5. [ ] Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has [_] been received. [_] not been received. [_] been filed in parent application Serial No. _____, filed on _____
6. [ ] Note the attached Examiner's Amendment.
7. [ ] Note the attached Examiner Interview Summary Record, PTOL-413.
8. [ ] Note the attached Examiner's Statement of Reasons for Allowance.
9. [ ] Note the attached NOTICE OF REFERENCES CITED, PTO-892.
10. [ ] Note the attached INFORMATION DISCLOSURE CITATION, PTO-1449.

PART II.

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE THREE MONTHS FROM THE "DATE MAILED" indicated on this form. Failure to timely comply will result in the ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

1. [ ] Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.
2. [X] APPLICANT MUST MAKE THE DRAWING CHANGES INDICATED BELOW IN THE MANNER SET FORTH ON THE REVERSE SIDE OF THIS PAPER.
   a. [X] Drawing informalities are indicated on the NOTICE RE PATENT DRAWINGS, PTO-948, attached hereto or to Paper No. 2 CORRECTION IS REQUIRED.
   b. [ ] The proposed drawing correction filed on _____ has been approved by the examiner. CORRECTION IS REQUIRED.
   c. [ ] Approved drawing corrections are described by the examiner in the attached EXAMINER'S AMENDMENT. CORRECTION IS REQUIRED.
   d. [ ] Formal drawings are now REQUIRED.

Any response to this letter should include in the upper right hand corner, the following information from the NOTICE OF ALLOWANCE AND ISSUE FEE DUE: ISSUE BATCH NUMBER, DATE OF THE NOTICE OF ALLOWANCE, AND SERIAL NUMBER.

Attachments:
- Examiner's Amendment
- Examiner Interview Summary Record, PTOL-413
- Reasons for Allowance
- Notice of References Cited, PTO-892
- Information Disclosure Citation, PTO-1449
- Notice of Informal Application, PTO-152
- Notice re Patent Drawings, PTO-948
- Listing of Bonded Draftsmen
- Other

JJ

ANDREW FAILES
SUPERVISORY PATENT
GROUP ART UNIT 2

PTOL-37 (REV. 2-95)

USCOMM-DC 85-3744

PTOL-85 (REV 4-86)

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

THOMAS E. SCHATZEL
3211 SCOTT BLVD., STE. 201
SANTA CLARA, CA 95054-3093

All communications regarding this application should give the serial number, date of filing, name of applicant, and batch number.

Please direct all communications to the Attention of "OFFICE OF PUBLICATIONS" unless advised to the contrary.

The application identified below has been examined and found allowable for issuance of Letters Patent. PROSECUTION ON THE MERITS IS CLOSED.

	SC/SERIAL NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT		DATE MAILED
	07/041,994	04/24/87	007	JACKSON JR, J	253	08/25/88
First Named Applicant	EKLUND,		KLAS H.			

TITLE OF INVENTION: HIGH VOLTAGE MOS TRANSISTORS

	ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
	SB-520-01	357-046.000	L66	UTILITY	YES	$280.00	11/25/88

The amount of the issue fee is specified in 37 C.F.R. 1.18. If the applicant qualified for and has filed a verified statement of small entity status in accordance with 37 C.F.R. 1.27, the issue fee is one-half the amount for non-small entities. The issue fee due printed above reflects applicant's status as of the time of mailing this notice. A verified statement of small entity status may be filed prior to or with payment of the issue fee. However, in accordance with 37 C.F.R. 1.28, failure to establish status as a small entity prior to or with payment of the issue fee precludes payment of the issue fee in the amount so established for small entities and precludes a refund of any portion thereof paid prior to establishing status as a small entity.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE as indicated above. The application shall otherwise be regarded as ABANDONED. The issue fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office. Where an authorization to charge the issue fee to a deposit account has been filed before the mailing of the notice of allowance, the issue fee is charged to the deposit account at the time of mailing of this notice in accordance with 37 C.F.R. 1.311. If the issue fee has been so charged, it is indicated above.

In order to minimize delays in the issuance of a patent based on this application, **this Notice may have been mailed prior to completion of final processing.** The nature and/or extent of the remaining revision or processing requirements may cause slight delays of the patent. In addition, **if prosecution is to be reopened, this Notice of Allowance will be vacated and the appropriate Office action will follow in due course.** If the issue fee has already been paid and prosecution is reopened, the applicant may request a refund or request that the fee be credited to a deposit account. However, *applicant may request* that the previously submitted issue fee be applied. If abandoned, applicant may request refund or credit to a deposit account.

In the case of each patent issuing without an assignment, the complete post office address of the inventor(s) will be printed in the patent heading and in the Official Gazette. If the inventor's address is now different from the address which appears in the application, please fill in the information in the spaces provided on PTOL-85b enclosed. If there are address changes for more than two inventors, enter the additional addresses on the reverse side of the PTOL-85b.

The appropriate spaces in the ASSIGNMENT DATA section of PTOL-85b must be completed in all cases. If it is desired to have the patent issue to an assignee, an assignment must have been previously submitted to the Patent and Trademark Office or must be submitted not later than the date of payment of the issue fee as required by 37 C.F.R. 1.334. Where there is an assignment, the assignee's name and address must be provided on the PTOL-85b to ensure its inclusion in the printed patent.

Advance orders for 10 or more printed copies of the prospective patent can be made by completing the information in Section 4 of PTOL-85b and submitting payment therewith. If use of a deposit account is being authorized for payment, PTOL-85c should also be forwarded. The order must be for at least 10 copies and must accompany the issue fee. The copies ordered will be sent only to the address specified in section 1 or 1A of PTOL-85b.

☒ Note attached communication from the Examiner.

☐ This notice is issued in view of applicant's communication filed _____

IMPORTANT REMINDER

Patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. See 37 CFR 1.20 (e)—(j).

PATENT AND TRADEMARK OFFICE COPY

8

Patent #8
11-10-88

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Eklund, Klas H.
Filed : 04/24/87
Examiner : Jackson Jr.,
Group Art Unit : 253
Atty Docket No.: SS-520-01
For : "HIGH VOLTAGE MOS TRANSISTORS"

Issue Batch No.: L66
Allowance Date 08/25/88
Serial No. : 07/041,994

Box Issue Fees
COMMISSIONER OF PATENTS
AND TRADEMARKS
Washington, D. C. 20231

Date of This Paper
October 19, 1988

FORMAL DRAWING TRANSMITTAL

Transmitted herewith are formal drawings for the above identified application as requested in the Notice of Allowance, Paper No. 7, mailed August 25, 1988. Corrections have been made as requested by the Examiner. Applicant respectfully requests that the formal drawings be filed.

Respectfully submitted,

By: _____
Thomas E. Schatzel
Reg. No. 22,614

Attorney for Applicant

LAW OFFICES OF THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard, Suite 201
Santa Clara, CA 95054-3093

Telephone: (408) 727-7077

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 10/19/88 (Date of Deposit)

Thomas E. Schatzel
Name of applicant, assignee, or Registered Rep.

Signature 10/19/88 Date

357 46

KLAS H. EKLUND
SS-520-01

Notice of Allowance: 08/25/88
Issue Batch No. : L66
Serial No. : 07/041,994
Filed : 04/24/87

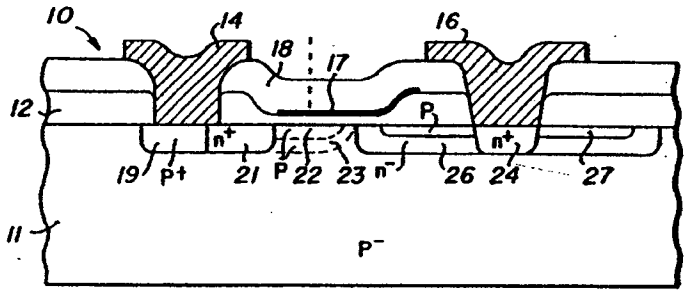

Fig_1

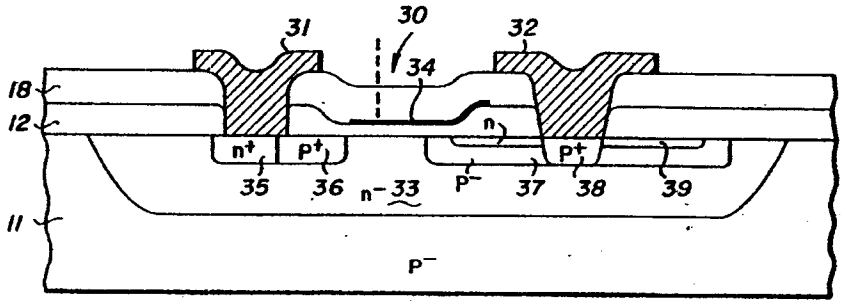

Fig_2

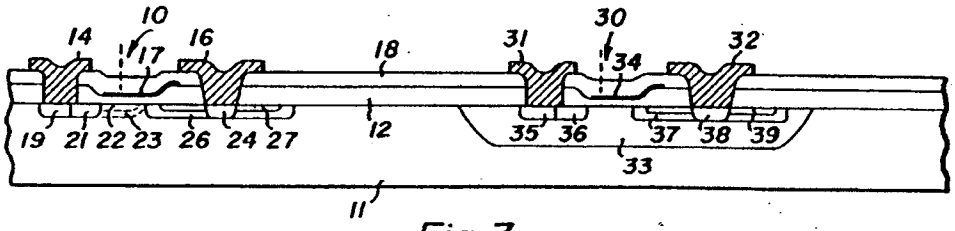

Fig_3

KLAS H. EKLUND
SS-520-01

Notice of Allowance: 08/25/88
Issue Batch No. : L66
ial No. : 07/041,994
Filed : 04/24/87

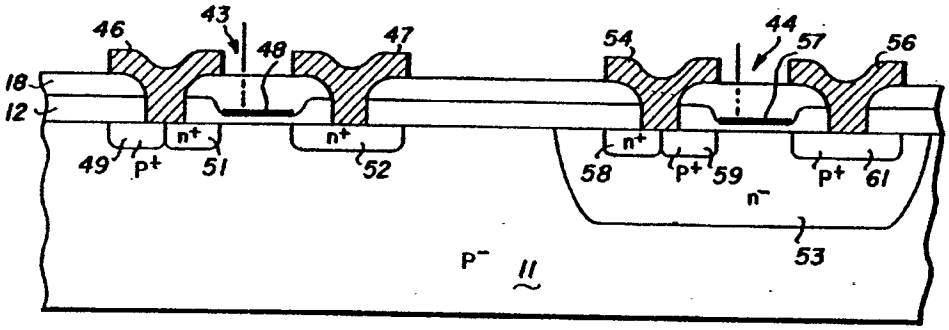

Fig_4

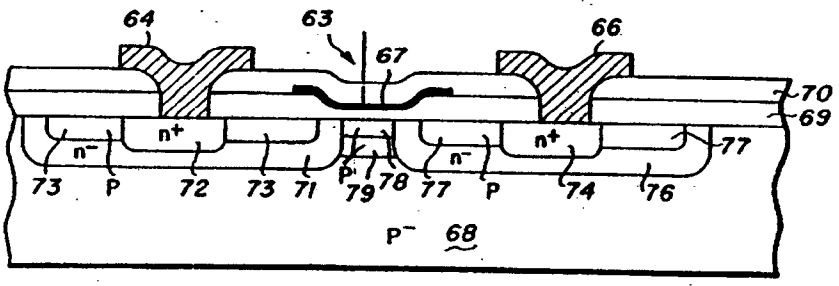

Fig_5

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Eklund, Klas H.
Filed : 04/24/87
Examiner : Jackson Jr., J.
Group Art Unit : 253
Atty Docket No.: SS-520-01
For : "HIGH VOLTAGE MOS TRANSISTORS"

Issue Batch No.: L66
Allowance Date 08/25/88
Serial No. : 07/041,994

Box Issue Fees
COMMISSIONER OF PATENTS
AND TRADEMARKS
Washington, D. C. 20231

Date of This Paper
October 19, 1988

PAYMENT OF ISSUE FEE (37 CFR 1.311)

1. Applicant hereby pays the issue fee.
2. Fee (37 CFR 1.18(a))
   Application status is:
   _X_ small entity- fee $ 280.00
   _X_ Verified Statement attached
   ____ Verified Statement filed
   ___ other than small entity- fee $ 560.00
3. Payment of fee
   _X_ Enclosed please find check 11177 for $ 302.00 *
   ___ Charge Deposit Account 19-0310 the sum of $ _____. A duplicate of this request is attached.

* Includes Advance Order and Assignment Recordal Fee

Respectfully submitted,

Thomas E. Schatzel
Reg. No. 22,611

Attorney for Applicant

Law Offices of THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard, Suite 201
Santa Clara, CA 95054-3093
Telephone: (408) 727-7077

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 10/19/88 (Date of Deposit)

Thomas E. Schatzel
Name of applicant, assignee, or Registered Representative

Signature 10/19/88 Date

PTOL-85b (REV. 4-86)

ISSUE FEE TRANSMITTAL

280 3469

U.S. Department of Commerce
Patent and Trademark Office

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PAT. & TRADEMARK OFFICE OCT 24 1988 MAIL ROOM

INVENTOR'S ADDRESS CHANGE | SC/SERIAL NO.

INVENTOR'S NAME

Street Address

City, State and ZIP Code

CO-INVENTOR'S NAME

Street Address

City, State and ZIP Code

☐ Check if additional changes are on reverse side.

MAILING INSTRUCTIONS

All further correspondence including the Issue Fee Receipt the Patent, and advanced orders will be mailed to the addressee entered in section 1 on PTOL-85c, unless you direct otherwise by specifying the appropriate name and address in 1A below. (Note: See box 5 below for correspondence concerning maintenance fee payments.)

2A. The COMMISSIONER OF PATENTS AND TRADEMARKS is requested to apply the Issue Fee to the application identified below.

(Signature of party in interest of record) (Date) 10/19/88

Note: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

	SC/SERIAL NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT		DATE MAILED
	07/041,994	04/24/87	007	JACKSON JR, J	253	08/25/88
First Named Applicant	EKLUND,	KLAS H.				

TITLE OF INVENTION: HIGH VOLTAGE MOS TRANSISTORS

	ATTY'S DOCKET NO.	CLASS/SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
	SB-520-01	357-046.000	L66	UTILITY	YES	$280.00	11/25/88

1A. Further correspondence to be mailed to the following:

Law Offices of THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard, Suite 201
Santa Clara, California 95054

2B. For printing on the patent front page, list the names of not more than 3 registered patent attorneys or agents OR, alternatively, the name of a firm having as a member a registered attorney or agent. If no name is listed, no name will printed.

1 LAW OFFICES OF
2 THOMAS E. SCHATZEL
3 A Prof. Corporation

DO NOT USE THIS SPACE

040 10/28/88 041994 1 242 280.00 CK
040 10/28/88 041994 1 501 15.00 CK

3. ASSIGNMENT DATA (print or type)

A. (1) ☐ This application is NOT assigned.
(2) ☐ Assignment previously submitted to the Patent and Trademark Office.
(3) ☒ Assignment submitted herewith.

B. For Printing On The Patent: (Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data below is only appropriate when an assignment has been previously submitted to the PTO or is submitted herewith. Completion of this form is NOT a substitute for filing of an assignment as required by 37 C.F.R. 1.334).

(1) NAME OF ASSIGNEE: POWER INTEGRATIONS, INC.

(2) ADDRESS: (City & State or Country) Mountain View California 94043

(3) STATE OF INCORPORATION, IF ASSIGNEE IS A CORPORATION: California

4. The following fees are enclosed: Ck. # 11177
XX Issue fee XX Advanced order ☒ Assignment recording

The following fees should be charged to deposit acc. no. 19-0310
(PTOL-85c or additional copy of PTOL-85b must be enclosed)

☐ Issue fee ☐ Assignment recording
☐ Advanced order ☒ Any additional fees due

Number of advanced order copies requested. 10
(must be for 10 or more copies)

5. All correspondence relating to maintenance fees will be addressed to the correspondence address unless a separate "Fee Address" is provided to the Patent and Trademark Office (37 C.F.R. 1.363). A "Fee Address" may be submitted by the owner of record with the payment of the issue fee or thereafter by using form PTO-1537.

TRANSMIT THIS FORM WITH FEE

PTO/SB/31 (4-96)

ISSUE FEE TRANSMITTAL

U.S. Department of Commerce
Patent and Trademark Office

This form is provided for formal transmittal and should be used for transmitting the Issue Fee. Sections 1A through 4 must be completed as appropriate.

INVENTOR(S) ADDRESS CHANGE | SC/SERIAL NO

INVENTOR'S NAME

Street Address

City, State and ZIP Code

CO INVENTOR'S NAME

Street Address

City, State and ZIP Code

☐ Check if additional changes are on reverse side.

MAILING INSTRUCTIONS

All further correspondence including the Issue Fee Receipt the Patent, and advanced orders will be mailed to the addressee entered in section 1 on PTOL-85c, unless you direct otherwise by specifying the appropriate name and address in 1A below. (Note: See box 5 below for correspondence concerning maintenance fee payments.)

2A. The COMMISSIONER OF PATENTS AND TRADEMARKS is requested to apply the Issue Fee to the application identified below.

(Signature of party in interest of record) | (Date) 10/19/88

Note: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

	SC/SERIAL NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT		DATE MAILED
	07/041,579	04/24/87	007	JACKSON JR, J	253	08/25/88
First Named Applicant	ERLING,		KLAS H.			

TITLE OF INVENTION: HIGH VOLTAGE MOS TRANSISTORS

	ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
	98-520-01	357-046.000	166	UTILITY	YES	$280.00	11/25/88

1A. Further correspondence to be mailed to the following:

Law Offices of THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard, Suite 201
Santa Clara, California 95054

2B. For printing on the patent front page, list the names of not more than 3 registered patent attorneys or agents OR, alternatively, the name of a firm having as a member a registered attorney or agent. If no name is listed, no name will printed.

1 LAW OFFICES OF
2 THOMAS E. SCHATZEL
3 A Prof. Corporation

DO NOT USE THIS SPACE

3. ASSIGNMENT DATA (print or type)

A. (1) ☐ This application is NOT assigned.
(2) ☐ Assignment previously submitted to the Patent and Trademark Office.
(3) ☒ Assignment submitted herewith.

B. For Printing On The Patent: (Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data below is only appropriate when an assignment has been previously submitted to the PTO or is submitted herewith. Completion of this form is NOT a substitute for filing of an assignment as required by 37 C.F.R. 1.334).

(1) NAME OF ASSIGNEE: POWER INTEGRATIONS, INC.

(2) ADDRESS: (City & State or Country) Mountain View California 94043

(3) STATE OF INCORPORATION, IF ASSIGNEE IS A CORPORATION: California

4. The following fees are enclosed: Ck. # 11177
☒ Issue fee ☒ Advanced order ☒ Assignment recording

The following fees should be charged to deposit acc. no. 19-0110
(PTOL-85c or additional copy of PTOL-85b must be enclosed)

☐ Issue fee ☐ Assignment recording
☐ Advanced order ☒ Any additional fees due

Number of advanced order copies requested: 10
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5. All correspondence relating to maintenance fees will be addressed to the correspondence address unless a seperate "Fee Address" is provided to the Patent and Trademark Office (37 C.F.R. 1.363). A "Fee Address" may be submitted by the owner of record with the payment of the issue fee or thereafter by using form PTO-1537.

TRANSMIT THIS FORM WITH FEE

9

pplicant or Patentee: Klas H. Eklund
erial or Patent No.: 07/041,994
iled or Issued: 04/24/87
or: "HIGH VOLTAGE MOS TRANSISTORS"

Attorney's Docket No. SS-520-01

MAIL ROOM OCT 24 1988 PAT. & TRADEMARK OFF.

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) and 1.27(c)) - SMALL BUSINESS CONCERN

#9

I hereby declare that I am

[ ] the owner of the small business concern identified below:
[X] an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN: POWER INTEGRATIONS, INC.
ADDRESS OF CONCERN: 411 Clyde Avenue
Mountain View, CA 94043

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled "HIGH VOLTAGE MOS TRANSISTORS" by inventor(s) Klas H. Eklund described in

[ ] the specification filed herewith
[X] application serial no. 07/041,994, filed April 24, 1987.
[ ] patent no. _____, issued _____.

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(d) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e). *NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

NAME: N/A
ADDRESS:
[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

NAME: N/A
ADDRESS
[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING: Klas H. Eklund
TITLE OF PERSON OTHER THAN OWNER: Vice President, Engineering
ADDRESS OF PERSON SIGNING: Power Integrations, Inc., 411 Clyde Avenue, Mountain View, California 94043
SIGNATURE: _____ DATE: 10/18/88

10

Atty. Docket No.: SS-510-01 #70

POWER OF ATTORNEY BY ASSIGNEE

The undersigned, as Assignee of the entire right, title, and interest in and to the subject matter which is described and claimed and for which a patent is sought on the invention entitled:

HIGH VOLTAGE MOS TRANSISTORS

the specification of which

☐ is attached hereto;

☒ was filed on April 24, 1987 as Application Serial No. 07/041,994 and was amended on 04/11/88; 08/15/88 (if applicable);

Assignment recorded on _____ (if applicable) at Reel/Frame _____

hereby elects to control the prosecution of this application and hereby appoints the following attorneys(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office in connection therewith:

Thomas E. Schatzel Reg. No. 22,611

Address all correspondence to:

LAW OFFICES OF THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard, Suite 201
Santa Clara, California 95054-3093

Address all telephone calls to Thomas E. Schatzel at telephone No. (408) 727-7077.

Assignee hereby petitions and requests that this file be closed to the inventor(s), or representative(s) thereof.

POWER INTEGRATIONS, INC.

Dated: 10/18/88

by _____
Klaus H. Eklund

Title: Vice President, Engineering

POWER INTEGRATIONS, INC.
411 Clyde Avenue
Mountain View, California 94043

U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

Paper No. 11

3 JAN 1989

253 4/24/87 041,994
Klas H. Eklund
High Voltage MOS Transistors

This is in response to the communication re the Power of Attorney filed 10/24/88

1. ☐ The power of attorney to you in this application has been revoked by the applicant.

2. ☐ In view of the notice in this application of the death of assignee, his power of attorney is terminated.

3. ☒ The power of attorney to you in this application has been accepted by the Commissioner of Patents & Trademarks.

For Director, Operation

4. ☐ The assignee in this application has intervened and appointed an attorney of his own selection. Further correspondence will be held with said attorney. (Rule 36, Rules of Practice.)

5. ☐ The revocation of the power of attorney to _____ has been entered and said attorney has been notified. Further correspondence will be addressed to you.

6. ☐ On _____, the applicant appointed assignee _____ as additional attorney in this application. Further correspondence will continue to be addressed to you as specified in the new power of attorney.

7. ☐ On _____, the applicant appointed assignee _____ as additional attorney in this application. Further correspondence will be addressed to said attorney. MPEP 403.02

8. ☐ The associate power of attorney to you in this application has been revoked by the attorney of record.

Thomas E. Schatzel

Law Offices of Thomas E. Schatzel, A Professional Corp.
3211 Scott Blvd., Ste. 201
Santa Clara, CA 95054-3093

L. Gilliatt
Director, Operation

RETAIN THIS COPY IN THE APPLICATION FILE

Copy A

FORM PTOL-305 (REV.9/75)

Attorney Docket No.: SS-520-01 PCO

PATENT & TRADEMARK OFFICE PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No.: 4,811,075

PATENT MAINTENANCE DIVISION

Granted: 03/07/89

Inventor(s): Klas H. Eklund

7041994

ENTERED BY PMD (12)

Box: Patent Address Change
Commissioner of Patents and Trademarks
Washington, D.C. 20231

CHANGE OF CORRESPONDENCE ADDRESS IN PATENT

Please

1. Change the address of the attorney(s) of record to:

Thomas E. Schatzel, Esq.
LAW OFFICES OF
THOMAS E. SCHATZEL
A PROFESSIONAL CORPORATION
16400 LARK AVENUE, SUITE 300
LOS GATOS, CA 95032

2. Change the correspondence address of the patent owner to:

_____

_____

_____

It is certified that the person whose signature appears below has the authority to change the correspondence address for the patent.

Date: 05/03/93

(Signature) THOMAS E. SCHATZEL

LAW OFFICES OF
THOMAS E. SCHATZEL
A PROFESSIONAL CORPORATION
16400 LARK AVENUE, SUITE 300
LOS GATOS, CA 95032

Tel. No.: (408) 358-7733

Reg. No.: 22,611
(If applicable)

- [ ] Inventor(s)
- [ ] Assignee of complete interest
- [X] Attorney or agent of record

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 05/03/93
(Date of Deposit)

Thomas E. Schatzel
Name of applicant, assignee or Registered Rep.

Signature 5/3/93 Date

THOMAS E. SCHATZEL
16400 LARK AVENUE, STE. 300
LOS GATOS, CA 95032

(Change of Correspondence Address in Patent [12-6])